REMARKS

Claims 1 through 17 are pending in this application, of which claims 6 through 17 stand withdrawn from consideration pursuant to the provisions of 37 C.F.R. § 1.142(b). Accordingly, claims 1 through 5 are active.

Claim 1 has been amended. Care has been exercised to avoid the introduction of new matter. Indeed, adequate descriptive support for the present Amendment should be apparent throughout the originally filed disclosure as, for example, Fig. 2F and the related discussion thereof in the written description of the specification. Applicants submit that the present Amendment does not generate any new matter issue.

Claims 1 through 5 were rejected under 35 U.S.C. § 102 for lack of novelty as evidenced by Gates et al.

In the statement of the rejection, the Examiner referred to Fig. 8 of Gates et al. asserting the disclosure of a semiconductor device corresponding to that claimed identifying, *inter alia*, etching stopper 56 and metal interconnect 74. This rejection is traversed.

The factual determination of lack of novelty under 35 U.S.C. § 102 requires the identical disclosure in a single reference of each element of a claimed invention such that the identically claimed invention is placed into the recognized possession of one having ordinary skill in the art. *Dayco Prods., Inc. v. Total Containment, Inc. 329 F.3d 1358, 66 USPQ2d 1801 (Fed. Cir. 2003); Crown Operations International Ltd. v. Solutia Inc., 289 F.3d 1367, 62 USPQ2d 1917 (Fed. Cir. 2002).* There is a significant structural difference between the claimed semiconductor device and the semiconductor device disclosed by Gates et al. that scotches the factual determination that Gates et al. disclose a semiconductor device identically corresponding to that claimed.

Specifically, independent claim 1 is directed to a semiconductor device comprising a multilayered film which includes first and second dielectric films separated by an etching stopper. A via plug and metal interconnect, which metal interconnect is formed on the via plug, are formed in the multilayered film. Claim 1 specifies that the upper surface of the etching stopper is located under the upper surface level of the metal interconnect, and the under surface of the etching stopper is located over the under surface level of the metal interconnect. No such structure is disclosed or suggested by Gates et al. Indeed, it should be apparent from Fig. 8 of Gates et al. relied upon by the Examiner, that the under surface of the etching stopper 56' is located under the under surface level of the metal interconnect - **not over** the under surface of the metal interconnect as in the claimed invention.

Applicants would point out that according to column 7 of Gates et al., lines 23 and 24, trench 20 may be a via, a line, or both. As depicted, the upper portion of trench 70 (Fig. 7) is wider than the low portion and, hence, element 74 in Fig. 8 would have been recognized by one having ordinary skill in the art as a dual damascene structural comprising a metal interconnect over a via plug. This is because one having ordinary skill in the art, following the disclosure of Gates et al., would separate the trench and via opening at a step as illustrated in Fig. 7. Thus, the metal interconnect would be located over the upper surface of the etching stopper layer 56' and the via plug would be located thereunder. In such a structure, the under surface of the etching stopper layer is located **under** the under surface level of the metal interconnect. But in the claimed invention, the under surface of the etching stopper layer is located **over** the under surface level of the metal interconnect.

The above argued structural difference between the claimed semiconductor device and the semiconductor device disclosed by Gates et al. is functionally significant. Specifically, as pointed

out in the paragraph bridging pages 5 and 6 of the written description of the specification, in accordance with the present invention a part of the region between adjacent interconnect lines in which the electric flux line converges is filled with a low dielectric constant material. Accordingly, substantial capacitance among the interconnect lines is reduced, even when a high dielectric constant material is employed as the etching stopper.

The above argued functionally significant structural difference between the claimed semiconductor device and the semiconductor disclosed by Gates et al. undermines the factual determination that Gates et al. disclose a semiconductor device identically corresponding to that claimed. *Minnesota Mining & Manufacturing Co. v. Johnson & Johnson Orthopaedics Inc., 976 F.2d 1559, 24 USPQ2d 1321 (Fed. Cir. 1992)*; *Kloster Speedsteel AB v. Crucible Inc., 793 F.2d 1565, 230 USPQ 81 (Fed. Cir. 1986)*. Applicants, therefore, submit that the imposed rejection of claims 1 through 5 under 35 U.S.C. § 102 for lack of novelty as evidenced by Gates et al. is not factually viable and, hence, solicit withdrawal thereof.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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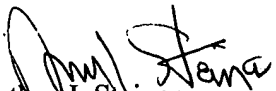

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